CLAIMS

What is claimed is:

1. An n-channel field effect transistor having a gate electrode in which at least a portion contacting a gate insulating film is made of a metal material having a work function close to the work function of n-type polysilicon.

2. An n-channel field effect transistor according to claim 1, wherein said metal material consists of a material selected from a group consisting of zirconium and hafnium.

3. An n-channel field effect transistor according to claim 1, wherein at least a portion of said gate electrode in contact with a gate insulating film is made of said metal material, and a portion other than said portion made of said metal material is made of a material having a predetermined low electrical resistivity.

4. A p-channel field effect transistor having a gate electrode in which at least a portion contacting a gate insulating film is made of a metal material having a work function close to the work function of p-type polysilicon.

5. A p-channel field effect transistor according to claim 4, wherein said metal material consists of a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

6. A p-channel field effect transistor according to claim 4, wherein said metal material consists of rhenium.

7. A p-channel field effect transistor according to claim 4, wherein at least a portion of said gate electrode in contact with a gate insulating film is made of said metal material, and a portion other than said portion made of said metal material is made of a material having a predetermined low electrical resistivity.

8. A complementary integrated circuit comprising:

an n-channel element having a gate electrode in which at least a portion contacting a gate insulating film is made of a first metal material having a work function close to the work function of n-type polysilicon; and

a p-channel element having a gate electrode in which at least a portion contacting a gate insulating film is made of a second metal material having a work function close to the work function of p-type polysilicon.

9. A complementary integrated circuit according to claim 8, wherein said first metal material consists of a material selected from a group consisting of zirconium and hafnium, and said second metal material consists of a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

10. A complementary integrated circuit according to claim 8, wherein said first metal material consists of a material selected from a group consisting of zirconium and hafnium, and said

second metal material consists of rhenium.

11. A complementary integrated circuit according to claim 8, wherein, in said gate electrode of said n-channel element, at least a portion of said gate electrode in contact with a gate insulating film is made of said first metal material, and a portion other than said portion made of said first metal material is made of a material having a predetermined low electrical resistivity, and

wherein, in said gate electrode of said p-channel element, at least a portion of said gate electrode in contact with a gate insulating film is made of said second metal material, and a portion other than said portion made of said second metal material is made of a material having a predetermined low electrical resistivity.

12. A method of manufacturing a complementary integrated circuit, comprising:

preparing a semiconductor substrate;

forming a region for forming an n-channel element and a region for forming a p-channel element on said semiconductor substrate via an element isolation region;

forming a dummy gate electrode in each of said region for forming an n-cannel element and said region for forming a p-channel element;

forming n-type diffusion regions in said region for forming an n-channel element and forming p-type diffusion regions in said region for forming a p-channel element;

forming an insulating film over the entire surface of said semiconductor substrate;

removing said dummy gate formed in one of said region for forming an n-channel element and said region for forming a p-channel element to form a first trench in said insulating film;

filling said first trench with a gate electrode material;

removing said dummy gate formed in the other of said region for forming an n-channel element and said region for forming a p-channel element to form a second trench in said insulating film; and

filling said second trench with a gate electrode material.

13. A method of manufacturing a complementary integrated circuit according to claim 12, wherein, in said forming n-type diffusion regions in said region for forming an n-channel element and forming p-type diffusion regions in said region for forming a p-channel element, an n-type impurity is ion implanted into said region for forming an n-channel element by using a resist film covering said region for forming a p-channel element and said dummy gate formed in said region for forming an n-channel element as a mask, and a p-type impurity is ion implanted into said region for forming a p-channel element by using a resist film covering said region for forming an n-channel element and said dummy gate formed in said region for forming a p-channel element as a mask.

14. A method of manufacturing a complementary integrated circuit according to claim 12, wherein, in said forming an insulating film over the entire surface of said semiconductor substrate, said insulating film is formed so as to cover said dummy gate formed in said region for forming an n-channel element and said dummy gate formed in said region for forming

a p-channel element; and said method further comprises, after said forming an insulating film over the entire surface of said semiconductor substrate, removing at least a potion of said insulating film to expose upper surfaces of said dummy gate formed in said region for forming an n-channel element and said dummy gate formed in said region for forming a p-channel element.

15. A method of manufacturing a complementary integrated circuit according to claim 12, wherein said method further comprises, after said removing said dummy gate formed in one of said region for forming an n-channel element and said region for forming a p-channel element to form a first trench in said insulating film, forming a gate insulating film at the bottom portion of said first trench, wherein, in said filling said first trench with a gate electrode material, said first trench is filled with said gate electrode material within said first trench and on said gate insulating film formed at the bottom portion of said first trench,

wherein said method further comprises, after said removing said dummy gate formed in the other of said region for forming an n-channel element and said region for forming a p-channel element to form a second trench in said insulating film, forming a gate insulating film at the bottom portion of said second trench, and wherein, in said filling said second trench with a gate electrode material, said second trench is filled with said gate electrode material within said second trench and on said gate insulating film formed at the bottom portion of said second trench.

16. A method of manufacturing a complementary integrated circuit according to claim 12, wherein, in said filling said first trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said first trench and is polished to expose the upper surface of said insulating film, and

wherein, in said filling said second trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said second trench and is polished to expose the upper surface of said insulating film.

17. A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of said gate electrode material portion, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of said gate electrode material portion.

18. A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench

comprises, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and

wherein a gate electrode material portion filling a trench formed in said region for forming an p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

19. A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity.

20. A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity.

21. A method of manufacturing a complementary integrated circuit, comprising:

preparing a semiconductor substrate;

forming a region for forming an n-channel element and a region for forming a p-channel element on said semiconductor substrate via an element isolation region;

forming an insulating film over the entire surface of said semiconductor substrate;

selectively removing said insulating film to form a first trench in said insulating film on one of said region for forming an n-channel element and said region for forming a p-channel element;

filling said first trench with a gate electrode material;

selectively removing said insulating film to form a second trench in said insulating film on the other of said region for forming an n-channel element and said region for forming a p-channel element;

filling said second trench with a gate electrode material;

removing said insulating film;

forming n-type diffusion regions in said region for forming an n-channel element and forming p-type diffusion regions in said region for forming a p-channel element.

22. A method of manufacturing a complementary integrated circuit according to claim 21, wherein said method further comprises, after said selectively removing said insulating film to form a first trench in said insulating film on one of said region for forming an n-channel element and said region for forming a p-channel element, forming a gate insulating film at the bottom portion of said first trench, wherein, in said filling said first trench with a gate electrode material, said first trench is filled with said gate electrode material within said first trench and on said gate insulating film formed at the bottom portion of said first trench,

wherein said method further comprises, after said selectively removing said insulating film to form a second trench in said insulating film on the other of said region for forming an n-channel element and said region for forming a p-channel element, forming a gate insulating film at the bottom portion of said second trench, and wherein, in said filling said second trench with a gate electrode material, said second trench is filled with said gate electrode material within said second trench and on said gate insulating film formed at the bottom portion of said second trench.

23. A method of manufacturing a complementary integrated circuit according to claim 21, wherein, in said filling said first trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said first trench and is polished to expose the upper surface of said insulating film, and

wherein, in said filling said second trench with a gate

electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said second trench and is polished to expose the upper surface of said insulating film.

24. A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of said gate electrode material portion, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of said gate electrode material portion.

25. A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and

wherein a gate electrode material portion filling a trench formed in said region for forming an p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel,

rhodium, palladium, rhenium and gold.

26. A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity.

27. A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity.